

IN THE CLAIMS

1. (Amended) A substrate bias generator of a semiconductor memory device having a voltage pump circuit to boost a substrate voltage in response to an input of an oscillating signal generated in an oscillator, said substrate bias generator further comprising:

a substrate voltage level detector having said substrate voltage input thereto and outputting a signal which drives said oscillator in response to a substrate voltage level detected by said substrate voltage level detector[, said substrate voltage level detector comprising:

a first MOS transistor having a channel connected to a power supply, said first MOS transistor being operated in response to a level of said substrate voltage, and

a second MOS transistor having a channel connected in series with a channel of said first MOS transistor and to a ground supply and having a gate connected to said substrate voltage]; and

a controller having input thereto a chip active enable signal, a self refresh mode enable signal, and an output signal of said substrate voltage level detector, said controller controlling a switching operation of said substrate voltage level detector in response to said substrate voltage level detected by said substrate voltage level detector, said controller also controlling said switching operation of said

substrate voltage level detector in response to said chip active enable signal and said self refresh mode enable signal such that said substrate voltage level detector is not operative to drive said oscillator during a stand-by state of a self-refresh mode of said semiconductor memory device.

3. (Amended) A substrate bias generator according to claim 2, wherein said controller comprises:

an inverter which inverts said self refresh enable signal;

a NOR circuit having [an] input [of] thereto said chip active enable signal and [having input thereto an inversion of] said inverted self refresh enable signal; and

an AND circuit having input thereto said output signal of said substrate voltage level detector and an output signal of said NOR circuit, said AND circuit controlling said first PMOS transistor.

4. (Amended) A substrate bias generator of a semiconductor memory device which performs refresh operations of memory cells according to a self refresh mode for refreshing said memory cells, said substrate bias generator comprising:

a voltage pump circuit to supply a negative voltage to a substrate;

an oscillator to drive said voltage pump circuit;  
a substrate voltage level detector to detect a level  
of said negative voltage and to drive said oscillator in  
response to said detected level; and

a controller circuit having input thereto a chip  
active enable signal, a self refresh mode enable signal, and  
an output of said substrate voltage level detector, an output  
of said controller circuit being input to said substrate  
voltage level detector, said output of said controller circuit  
being responsive to said chip active enable signal and said  
self refresh mode enable signal such that said substrate  
voltage level detector is not operative to drive said  
oscillator during a stand-by state of said self refresh mode  
of said semiconductor memory device;

said substrate voltage level detector comprising:

a PMOS transistor having a gate coupled to said  
output of said controller circuit and having a  
source coupled to a power supply terminal, and

a MOS transistor having a gate connected to  
said negative voltage, and a channel connected in  
series with a channel of said PMOS transistor and  
between said power supply terminal and a ground  
supply, said MOS transistor being operated in  
response to a level of said negative voltage,